CLAIMS

1. An integrated circuit, comprising: a voltage generator supplying a determined voltage, and a voltage-limiting circuit arranged at the output of the voltage generator, the voltage-limiting circuit comprising:

at least one PN junction formed by a diode-arranged MOS transistor, said PN junction having a breakdown voltage defining a threshold for triggering the voltage-limiting circuit as from which the PN junction is on by avalanche effect,

at least one load in series with the PN junction, for limiting an avalanche current passing through the PN junction when the PN junction is on, and

at least one switch in parallel with the PN junction and the load, arranged for being in the open state when the PN junction is off and in the closed state when the PN junction is on.

2. The integrated circuit of claim 1 wherein the load is chosen such that the avalanche current passing through the PN junction is at least two times lower than a current passing through the switch when the voltage-limiting circuit is triggered.

3. The integrated circuit of claim 1 wherein the load comprises a MOS transistor.

4. The Integrated circuit of claim 1 wherein the switch comprises a MOS transistor.

5. The integrated circuit of claim 4 wherein the switch comprises an NMOS transistor, the gate of which is linked to one terminal of the PN junction through an inverter.

6. The integrated circuit of claim 4 wherein the switch comprises a PMOS transistor, the gate of which is connected to one terminal of the PN junction.

7. The integrated circuit of claim 1 wherein the switch comprises a MOS transistor, the load comprises a MOS transistor, the MOS transistor of the switch is current-mirror arranged with the MOS transistor of the load.

8. The integrated circuit of claim 1 wherein the voltage generator comprises a booster circuit.

9. The integrated circuit of claim 1, comprising a circuit for delivering a halt signal for stopping the voltage generator when the voltage-limiting circuit is triggered.

10. The integrated circuit of claim 9 wherein said circuit for delivering a halt signal comprises an inverting circuit, the input of which is linked to one point of the voltage-limiting circuit, and a logic gate having one input linked to the output of the inverting circuit, the logic gate adapting the voltage of the logic signal from a voltage to be regulated present in the limiting circuit to a logic signal voltage.

11. A voltage generator, comprising:

a voltage generator circuit having an output;

a load coupled to the output;

a diode structure having a first terminal coupled to the load at a node and a second terminal coupled to a reference potential; and

a switch coupled to the output and to the reference potential, the switch having a control terminal coupled to the node.

12. The generator of claim 1 wherein the diode is configured to have a breakdown voltage, and the load is structured such that current passing through the diode structure is at least twice the current passing through the switch when the breakdown voltage is exceeded in the diode structure.

13. A voltage generator, comprising:

a voltage generator circuit having an output;

a first MOS transistor coupled to the output and to a node, the MOS transistor having a gate also coupled to the node;

a second MOS transistor coupled to the node and to a ground reference potential, the second MOS transistor having a gate coupled to the ground reference potential; and

a third MOS transistor coupled to the output and to a fourth MOS transistor, the third MOS transistor having a gate coupled to the node and the fourth MOS transistor coupled to the ground reference potential and having a gate coupled to a voltage source, the third MOS transistor is current-mirror arranged with the first MOS transistor.

14. The generator of claim 13 wherein the width-to-length ratio of the first MOS transistor is lower than 1, and the third MOS transistor has a width-to-length ratio greater than 10.

15. The generator of claim 13 wherein the first and second MOS transistors form a trigger stage and the third and fourth MOS transistors form a limiting stage, and further wherein the ratio of current flowing in the limiting stage is proportional to the current in the trigger stage in a range of 2-to-1 to 100-to-1.

16. A voltage generator, comprising:

a voltage generator circuit having an output;

a first resistive element coupled to the output and to a first node;

a first MOS transistor coupled to the resistor and a ground reference potential, the second MOS transistor having a gate coupled to the ground reference potential;

a second MOS transistor coupled to the output and to a second node, the second MOS transistor having a gate coupled to the first node;

a second resistive element coupled to the second node and to the ground reference potential; and

a third MOS transistor coupled to the output and to the ground reference potential and having a gate terminal coupled to the second node.

17. The generator of claim 16 wherein the first resistive element and the first MOS transistor form a trigger stage and the second MOS transistor, second resistive element, and third MOS transistor form a limiting stage, and wherein the ratio of current in the trigger stage to the current in the limiting stage is in the range of 2-to-1 to 100-to-1.

18. The generator of claim 16 wherein the first and third MOS transistors comprise NMOS transistors and the second MOS transistor comprises a PMOS transistor.

19. A voltage generator, comprising:

a voltage generator circuit having an output;

a first MOS transistor coupled to the output and to a first node and having a gate terminal coupled to a first voltage source;

a diode structure coupled to the first node and a ground reference potential;

a second MOS transistor coupled to the output and the ground reference potential and having a gate terminal coupled to the first node;

a third MOS transistor coupled to the output and to a second node and having a gate terminal coupled to the first node;

a first resistive element coupled to the second node and to the ground reference potential; and

an inverter coupled to the second node and having an output terminal.

20. The generator of claim 19 wherein the output terminal is coupled to the generator circuit to shut off the generator circuit when the breakdown voltage of the first MOS transistor is exceeded.

21. A voltage generator, comprising:

a voltage generating circuit adapted to generate an output voltage on an output thereof;

a trigger stage coupled between the output and a reference potential, the trigger stage configured to couple the output to the reference potential when the output voltage reaches a breakdown voltage; and

a limiting stage coupled between the output and the reference potential and to the trigger stage, the limiting stage limiting current in the trigger stage when the output voltage reaches the breakdown voltage.

22. The generator of claim 21 wherein the trigger stage comprises a PN junction that conducts an avalanche current when the breakdown voltage is reached at the output.

23. The generator of claim 22 wherein the limiting circuit comprises a switch that is turned on when the PN junction conducts, the switch configured to conduct a current greater than the avalanche current.

24. The generator of claim 21, further comprising a circuit for generating an off signal to the voltage generating circuit when the PN junction conducts the avalanche current and for generating an on signal to the voltage generating circuit when the PN junction does not conduct the avalanche current.

25. A method for regulating a voltage generator having a voltage generating circuit adapted to generate a determined voltage on an output, the method comprising:

providing a PN junction and a load coupled in series between the output and a reference potential that conduct an avalanche current when voltage on the output reaches a breakdown voltage of the PN junction; and

turning on a switch, which is coupled in parallel with the series-connected PN junction and load between the reference potential and the output, when the PN junction conducts the avalanche current to limit the avalanche current in the PN junction so that the avalanche current is at least two times lower than current flowing through the switch, and turning off the switch when the PN junction does not conduct the avalanche current.

26. The method of claim 25, further comprising generating an off signal to the voltage generating circuit from an on/off signal generating circuit when the PN junction conducts avalanche current and generating an on signal to the voltage generating circuit when the PN junction is not conducting an avalanche current.

27. The method of claim 25, further comprises providing the switch to have a width-to-length ratio such that the switch conducts greater current than the avalanche current in the PN junction.

28. The method of claim 27 wherein providing the PN junction and providing the switch comprises configuring the PN junction and configuring the switch

such that the ratio of current in the switch to the avalanche current is in the range of 2-to-1 to 100-to-1.